Remarks

The present amendment is made in response to the non-final Office Action dated January 13, 2006, and identified as Paper No. 010906. Claims 7-10 are pending.

In the Action, the Examiner rejected claims 7-10 under 35 U.S.C. § 112, second paragraph as indefinite due to the use of the word "predetermined." Claims 7-9 were rejected under 35 U.S.C. § 102(b) as anticipated by Japanese Patent Reference No. 01-222,450 to Kobayashi ("*Kobayashi*"). Claims 7-8 and 10 were rejected under 35 U.S.C. § 102(b) as anticipated by Japanese Patent Reference No. 2002-319,558 to Naito ("*Naito*"). Claims 7-10 were rejected under 35 U.S.C. § 102(b) as anticipated by Japanese Patent Reference No. 02-239,621 to Nakamura ("*Nakamura*").

I. Rejection under 35 U.S.C. § 112, second paragraph

Although the use of predetermined is fully explained in the specification and well know to those of ordinary skill in the art, Applicant has amended claim 7 to remove the reference.

II. Rejections under 35 U.S.C. § 102(b)

Applicant has amended claim 7 to further recite the step of forming the socket plate by; providing a base plate having a chemical vapor deposition layer thereon; coating said deposition layer with a positive resist material; exposing said resist material with a second pattern corresponding to said first pattern; etching said deposition layer using said resist material as a mask; removing said resist material; etching said base plate to form a plurality of cavities arranged in said second pattern; and removing said deposition layer;. As explained in paragraph [0019] of the specification, the socket plate may be formed through a silicon etching processing using a mask having a pattern corresponding to the mask pattern used to form the solder bumps prior to the grinding steps. In fact, the same mask may be used (by inverting it) to form the

cavities and the solder bumps, so that when the solder bumps are positioned over the plate, each bump may be inserted into one of the cavities. While the references cited by the Examiner are in Japanese, none of the references cited by the Examiner appear to disclose the formation of cavities corresponding to the solder bumps by using etching process and a mask having a pattern that corresponds to the solder bump mask (or is the same mask). For example, *Kobayashi* discloses a grid of grooves rather than cavities for accepting circuitry rather than solder bumps, *Naito* discloses slots where the entire chip package may be received, and *Nakamura* discloses a line of parallel grooves for receiving the circuitry. Accordingly, none of these references discloses the claimed cavities, each of which receives one of the corresponding solder bumps, and therefore none of the reference disclose preparing the socket plate according to etching process recited in claim 7 that forms the corresponding cavities prior to attaching the wafer to the chuck and grinding the rear surface.

Applicant grants authorization to charge any fees in regard to this response to Deposit Account No. 50-1546. In view of the foregoing, the Examiner's reconsideration and allowance of the claims of the present application is believed to be in order. If the Examiner believes a phone conference with Applicant's attorney would expedite prosecution of this application, please contact the undersigned at (315) 218-8515.

Respectfully submitted,

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